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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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**TRANSMITTAL
FORM**

Application Number

09/802,289

Filing Date

March 8, 2001

First Named Inventor

Ashley Saulsbury

Group Art Unit

Examiner Name

Total Number of Pages in This Submission

Attorney Docket Number

16747-010010US

ENCLOSURES (check all that apply)☐ Fee Transmittal Form☐ Fee Attached☐ Amendment / Response☐ After Final☐ Affidavits/declaration(s)☐ Extension of Time Request☐ Express Abandonment Request☒ Third Information Disclosure
Statement Under 37 CFR §1.97 and
§1.98☐ Certified Copy of Priority
Document(s)☐ Response to Missing Parts/
Incomplete Application☐ Response to Missing
Parts under 37 CFR
1.52 or 1.53☐ Assignment Papers
(for an Application)☐ Drawing(s)☐ Licensing-related Papers☐ Petition Routing Slip (PTO/SB/69)
and Accompanying Petition☐ Petition to Convert to a
Provisional Application☐ Power of Attorney, Revocation
Change of Correspondence Address☐ Terminal Disclaimer☐ Request for Refund☐ CD, Number of CD(s)☐ After Allowance Communication to
Group☐ Appeal Communication to Board of
Appeals and Interferences☐ Appeal Communication to Group
(Appeal Notice, Brief, Reply Brief)☐ Proprietary Information☐ Status Letter☒ Return Postcard☒ Other Enclosure(s)
(please identify below):Copies of five (5) cited
references

Remarks

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Chad S. Hilyard Reg. No. 40,647

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Date

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Jennifer Gallant

Date

12/11/01

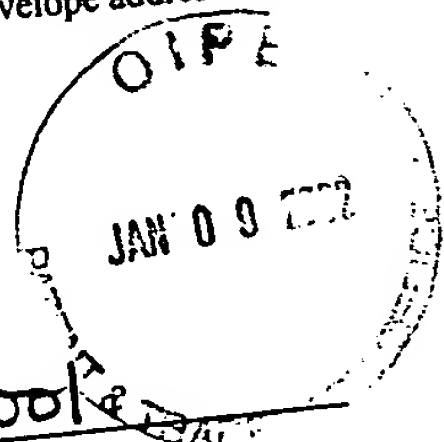
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Client Reference No.: P2405/US



On December 11, 2001

TOWNSEND and TOWNSEND and CREW LLP

By: Jennifer Hallant

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Ashley Saulsbury et al.

Application No.: 09/802,289

Filed: March 8, 2001

For: VLIW Computer Processing
Architecture Having a Scalable Number of
Register Files

Examiner: Unassigned

Art Unit: 2131

THIRD INFORMATION DISCLOSURE
STATEMENT UNDER 37 CFR §1.97 and
§1.98

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of the references are enclosed. Also enclosed is a copy of the Search/Examination report corresponding to the PCT application. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement, since it is being submitted prior to the first Office Action. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,



Chad S. Hilyard
Reg. No. 40,647

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PTO/SB/08B (08-00)

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Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known

Application Number	09/802,289
Filing Date	March 8, 2001
First Named Inventor	Saulsbury, Ashley
Group Art Unit	2131
Examiner Name	
Attorney Docket Number	016747-010010US

Sheet 3 of

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

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	A	NUMOMURA Y ET AL: "M32R/D-INTEGRATING DRAM AND MICROPROCESSOR" IEEE MICRO, IEEE INC. NEW YORK, US, vol. 17 no. 6, 1 November 1997 (1997-11-01), pages 40-48, XP000726003; ISSN: 0272-1732.	
	B	KOZYRAKIS C E ET AL: "SCALABLE PROCESSORS IN THE BILLION-TRANSISTOR ERA: IRAM" COMPUTER, IEEE COMPUTER SOCIETY, LONG BEACH, CA, US, vol. 20, no. 0 1 September 1997 (1997-09-01), pages 75- 78, XP000730003; ISSN: 0018-9162.	
	C	HERRMANN KLAUS, HILGENSTOCK JOERG, PIRSCH PETER: "ARCHITECTURE OF A MULTIPROCESSOR SYSTEM WITH EMBEDDED DRAM FOR LARGE AREA INTEGRATION" 8 October 1997 (1997-10-08), IEEE INTERNATIONAL CONFERENCE ON INNOVATIVE SYSTEMS IN SILICON, PISCATAWAY, NJ, USA; XP002179990	

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